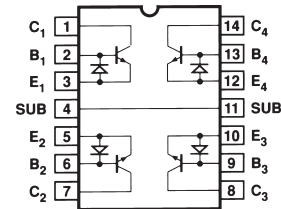


### FEATURES

- Low Offset Voltage: 200  $\mu\text{V}$  max
- High Current Gain: 400 min
- Excellent Current Gain Match: 2% max
- Low Noise Voltage at 100 Hz, 1 mA:  $2.5 \text{ nV}/\sqrt{\text{Hz}}$  max
- Excellent Log Conformance:  $r_{BE} = 0.6 \Omega$  max
- Matching Guaranteed for All Transistors
- Available in Die Form

### PIN CONNECTIONS

- 14-Lead Cerdip (Y Suffix)
- 14-Lead Plastic DIP (P Suffix)
- 14-Lead SO (S Suffix)



### PRODUCT DESCRIPTION

The MAT04 is a quad monolithic NPN transistor that offers excellent parametric matching for precision amplifier and nonlinear circuit applications. Performance characteristics of the MAT04 include high gain (400 minimum) over a wide range of collector current, low noise ( $2.5 \text{ nV}/\sqrt{\text{Hz}}$  maximum at 100 Hz,  $I_C = 1 \text{ mA}$ ) and excellent logarithmic conformance. The MAT04 also features a low offset voltage of 200  $\mu\text{V}$  and tight current gain matching, to within 2%. Each transistor of the MAT04 is individually tested to data sheet specifications. For matching parameters (offset voltage, input offset current, and gain match), each of the dual transistor combinations are

verified to meet stated limits. Device performance is guaranteed at 25°C and over the industrial and military temperature ranges.

The long-term stability of matching parameters is guaranteed by the protection diodes across the base-emitter junction of each transistor. These diodes prevent degradation of beta and matching characteristics due to reverse bias base-emitter current.

The superior logarithmic conformance and accurate matching characteristics of the MAT04 makes it an excellent choice for use in log and antilog circuits. The MAT04 is an ideal choice in applications where low noise and high gain are required.

### REV. D

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# MAT04—SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

(@  $T_A = 25^\circ\text{C}$  unless otherwise noted. Each transistor is individually tested. For matching parameters ( $V_{OS}$ ,  $I_{OS}$ ,  $\Delta h_{FE}$ ) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.)

Parameter	Symbol	Conditions	MAT04E			MAT04F			Unit
			Min	Typ	Max	Min	Typ	Max	
Current Gain	$h_{FE}$	$10\ \mu\text{A} \leq I_C \leq 1\ \text{mA}$ $0\ \text{V} \leq V_{CB} \leq 30\ \text{V}^1$	400	800		300	600		
Current Gain Match	$\Delta h_{FE}$	$I_C = 100\ \mu\text{A}$ $0\ \text{V} \leq V_{CB} \leq 30\ \text{V}^2$		0.5	2		1	4	%
Offset Voltage	$V_{OS}$	$10\ \mu\text{A} \leq I_C \leq 1\ \text{mA}$ $0\ \text{V} \leq V_{CB} \leq 30\ \text{V}^3$		50	200		100	400	$\mu\text{V}$
Offset Voltage Change vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	$10\ \mu\text{A} \leq I_C \leq 1\ \text{mA}$ $V_{CB} = 0\ \text{V}^3$		5	25		10	50	$\mu\text{V}$
Offset Voltage Change vs. $V_{CB}$	$\Delta V_{OS}/\Delta V_{CB}$	$10\ \mu\text{A} \leq I_C \leq 1\ \text{mA}$ $0\ \text{V} \leq V_{CB} \leq 30\ \text{V}^3$		50	100		100	200	$\mu\text{V}$
Bulk Emitter Resistance	$r_{BE}$	$10\ \mu\text{A} \leq I_C \leq 1\ \text{mA}$ $V_{CB} = 0\ \text{V}^4$		0.4	0.6		0.4	0.6	$\Omega$
Input Bias Current	$I_B$	$I_C = 100\ \mu\text{A}$ $0\ \text{V} \leq V_{CB} \leq 30\ \text{V}$		125	250		165	330	nA
Input Offset Current	$I_{OS}$	$I_C = 100\ \mu\text{A}$ ; $V_{CB} = 0\ \text{V}$		0.6	5		2	13	nA
Breakdown Voltage	$BV_{CEO}$	$I_C = 10\ \mu\text{A}$	40			40			V
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_B = 100\ \mu\text{A}$ ; $I_C = 1\ \text{mA}$		0.03	0.06		0.03	0.06	V
Collector-Base Leakage Current	$I_{CBO}$	$V_{CB} = 40\ \text{V}$		5			5		pA
Noise Voltage Density	$e_n$	$V_{CB} = 0\ \text{V}$ ; $f_O = 10\ \text{Hz}$		2	3		2	4	$\text{nV}/\sqrt{\text{Hz}}$
		$I_C = 1\ \text{mA}$ ; $f_O = 100\ \text{Hz}$		1.8	2.5		1.8	3	$\text{nV}/\sqrt{\text{Hz}}$
		$f_O = 1\ \text{kHz}^5$		1.8	2.5		1.8	3	$\text{nV}/\sqrt{\text{Hz}}$
Gain Bandwidth Product	$f_T$	$I_C = 1\ \text{mA}$ ; $V_{CE} = 10\ \text{V}$		300			300		MHz
Output Capacitance	$C_{OBO}$	$V_{CB} = 15\ \text{V}$ ; $I_E = 0$ $f = 1\ \text{MHz}$		10			10		pF
Input Capacitance	$C_{EBO}$	$V_{BE} = 0\ \text{V}$ ; $I_C = 0$ $f = 1\ \text{MHz}$		40			40		pF

### NOTES

<sup>1</sup>Current gain measured at  $I_C = 10\ \mu\text{A}$ ,  $100\ \mu\text{A}$  and  $1\ \text{mA}$ .

<sup>2</sup>Current gain match is defined as:  $\Delta h_{FE} = \frac{100(\Delta I_B)(h_{FE}^{MIN})}{I_C}$

<sup>3</sup>Measured at  $I_C = 10\ \mu\text{A}$  and guaranteed by design over the specified range of  $I_C$ .

<sup>4</sup>Guaranteed by design.

<sup>5</sup>Sample tested.

Specifications subject to change without notice.

**ELECTRICAL CHARACTERISTICS** (at  $-25^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  for MAT04E,  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  for MAT04F, unless otherwise noted. Each transistor is individually tested. For matching parameters ( $V_{OS}$ ,  $I_{OS}$ ) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.)

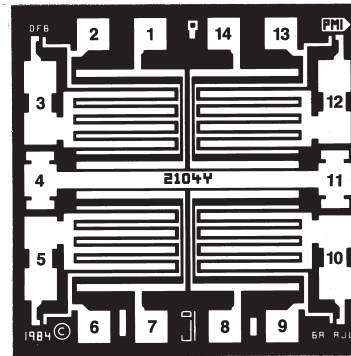
Parameter	Symbol	Conditions	MAT04E			MAT04F			Unit
			Min	Typ	Max	Min	Typ	Max	
Current Gain	$h_{FE}$	$10\ \mu\text{A} \leq I_C \leq 1\ \text{mA}$ $0\ \text{V} \leq V_{CB} \leq 30\ \text{V}^1$	225	625		200	500		
Offset Voltage	$V_{OS}$	$10\ \mu\text{A} \leq I_C \leq 1\ \text{mA}$ $0\ \text{V} \leq V_{CB} \leq 30\ \text{V}^2$		60	260	120	520	$\mu\text{V}$	
Average Offset Voltage Drift	$\text{TCV}_{OS}$	$I_C = 100\ \mu\text{A}$ $V_{CB} = 0\ \text{V}^3$		0.2	1	0.4	2	$\mu\text{V}/^{\circ}\text{C}$	
Input Bias Current	$I_B$	$I_C = 100\ \mu\text{A}$ $0\ \text{V} \leq V_{CB} \leq 30\ \text{V}$		160	445	200	500	nA	
Input Offset Current	$I_{OS}$	$I_C = 100\ \mu\text{A}$ $V_{CB} = 0\ \text{V}$		4	20	8	40	nA	
Average Offset Current Drift	$\text{TCI}_{OS}$	$I_C = 100\ \mu\text{A}$ $V_{CB} = 0\ \text{V}$		50		100		$\text{pA}/^{\circ}\text{C}$	
Breakdown Voltage Collector-Base	$\text{BV}_{CEO}$	$I_C = 10\ \mu\text{A}$	40			40		V	
Leakage Current Collector-Base	$I_{CBO}$	$V_{CB} = 40\ \text{V}$		0.5		0.5		nA	
Leakage Current Collector-Emitter	$I_{CES}$	$V_{CE} = 40\ \text{V}$		5		5		nA	
Leakage Current Collector-Substrate	$I_{CS}$	$V_{CS} = 40\ \text{V}$		0.7		0.7		nA	

# MAT04

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

Collector-Base Voltage ( $BV_{CBO}$ )	40 V
Collector-Emitter Voltage ( $BV_{CEO}$ )	40 V
Collector-Collector Voltage ( $BV_{CC}$ )	40 V
Emitter-Emitter Voltage ( $BV_{EE}$ )	40 V
Collector Current	30 mA
Emitter Current	30 mA
Substrate (Pin-4 to Pin-11) Current	30 mA
Operating Temperature Range	
MAT04EY	-25°C to +85°C
MAT04FY, FP, FS	-40°C to +85°C
Storage Temperature	
Y Package	-65°C to +150°C
P Package	-65°C to +125°C
Lead Temperature (Soldering, 60 sec)	+300°C

## DICE CHARACTERISTICS



1. Q1 COLLECTOR
2. Q1 BASE
3. Q1 EMITTER
4. SUBSTRATE
5. Q2 EMITTER
6. Q2 BASE
7. Q2 COLLECTOR
8. Q3 COLLECTOR
9. Q3 BASE
10. Q3 EMITTER
11. SUBSTRATE
12. Q4 EMITTER
13. Q4 BASE
14. Q4 COLLECTOR

Die Size 0.060 × 0.060 Inch, 3600 Sq. mm  
(1.52 × 1.52 mm, 2.31 sq. mm)

Package Type	$\theta_{JA}^2$	$\theta_{JC}$	Units
14-Lead Cerdip	108	16	°C/W
14-Lead Plastic DIP	83	39	°C/W
14-Lead SO	120	36	°C/W

## NOTES

<sup>1</sup>Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

<sup>2</sup> $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for cerdip and P-DIP packages;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SO package.

## ORDERING GUIDE

Model	$T_A = 25^\circ\text{C}$ $V_{OS\ max}$	Temperature Range	Package Description	Package Option
MAT04EY*	200 $\mu\text{V}$	-25°C to +85°C	Cerdip	Q-14
MAT04FY*	400 $\mu\text{V}$	-40°C to +85°C	Cerdip	Q-14
MAT04FP	400 $\mu\text{V}$	-40°C to +85°C	P-DIP-14	N-14
MAT04FS	400 $\mu\text{V}$	-40°C to +85°C	14-Lead SO	SO-14

## NOTES

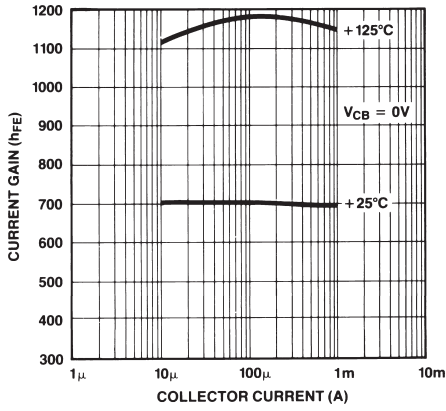
\*Not for new designs; obsolete April 2002.

## CAUTION

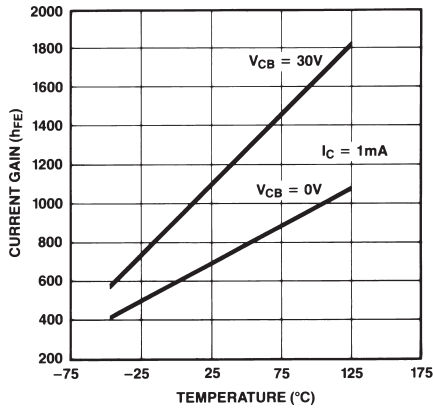
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the MAT04 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



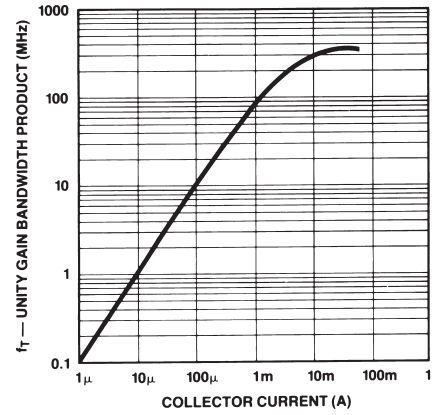
# Typical Performance Characteristics—MAT04



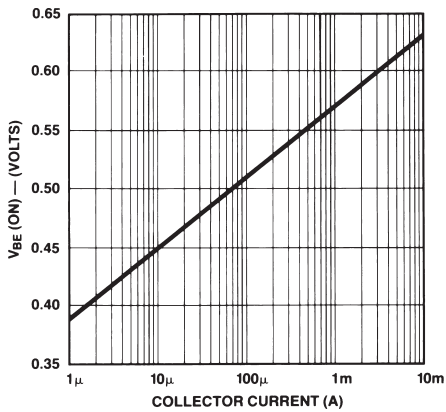
TPC 1. Current Gain vs. Collector Current



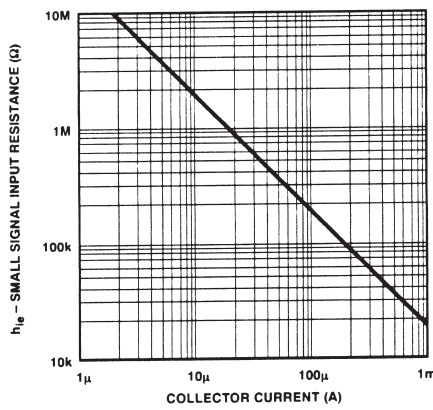
TPC 2. Current Gain vs. Temperature



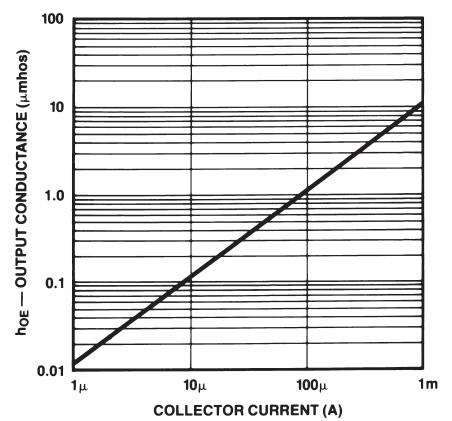
TPC 3. Gain Bandwidth vs. Collector Current



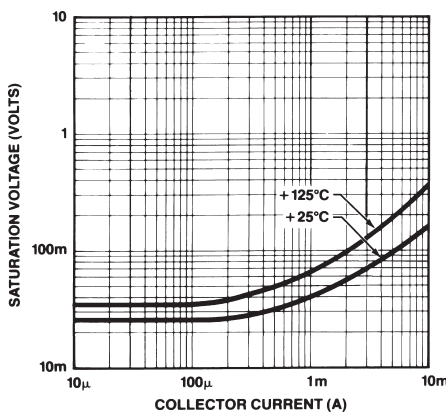
TPC 4. Base-Emitter-On-Voltage vs. Collector Current



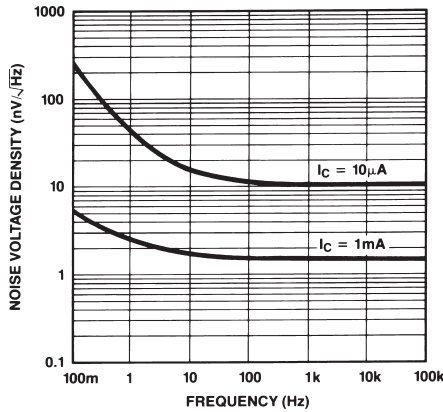
TPC 5. Small Signal Input Resistance ( $h_{ie}$ ) vs. Collector Current



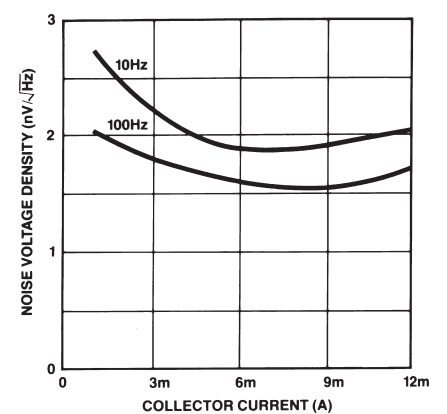
TPC 6. Small Signal Output Conductance vs. Collector Current



TPC 7. Saturation Voltage vs. Collector Current

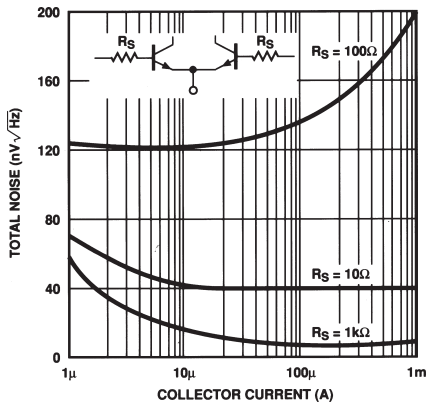


TPC 8. Noise Voltage Density vs. Frequency

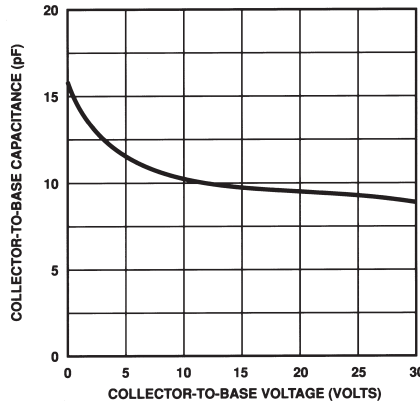


TPC 9. Noise Voltage Density vs. Collector Current

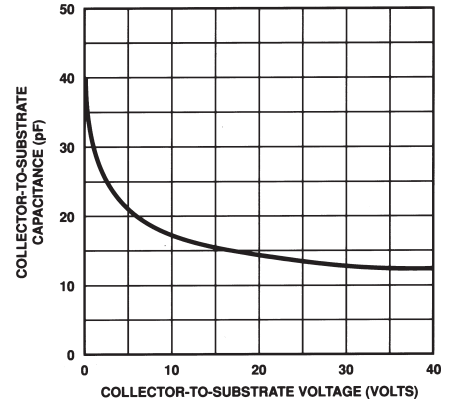
# MAT04



TPC 10. Total Noise vs. Collector Current



TPC 11. Collector-to-Base Capacitance vs. Collector-to-Base Voltage



TPC 12. Collector-to-Substrate Capacitance vs. Collector-to-Substrate Voltage

## APPLICATION NOTES

It is recommended that one of the substrate pins (Pins 4 and 11) be tied to the most negative circuit potential to minimize coupling between devices. Pins 4 and 11 are internally connected.

## APPLICATIONS

### CURRENT SOURCES

The MAT04 can be used to implement a variety of high impedance current mirrors as shown in Figures 1, 2, and 3. These current mirrors can be used as biasing elements and load devices for amplifier stages.

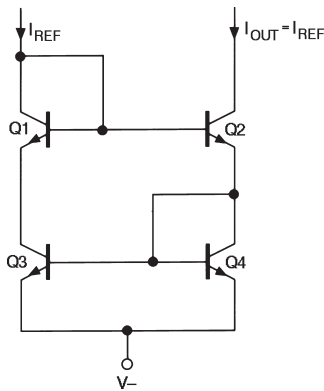


Figure 1. Unity Gain Current Mirror,  $I_{OUT} = I_{REF}$

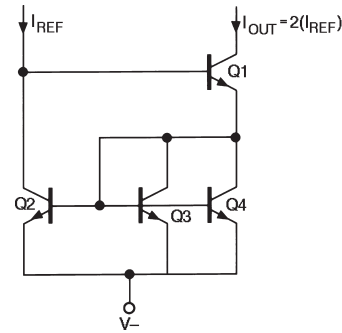


Figure 2. Current Mirror,  $I_{OUT} = 2(I_{REF})$

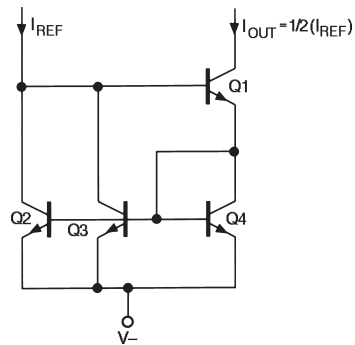


Figure 3. Current Mirror,  $I_{OUT} = 1/2(I_{REF})$

The unity-gain current mirror of Figure 1 has an accuracy of better than 1% and an output impedance of over 100 MΩ at 100 μA. Figures 2 and 3 show modified current mirrors designed for a current gain of two, and one-half respectively. The accuracy of these mirrors is reduced from that of the unity-gain source due to base current errors but is still better than 2%.

Figure 4 is a temperature independent current sink that has an accuracy of better than 1% at an output current of 100 μA to 1 mA. The Schottky diode acts as a clamp to ensure correct circuit start-up at power on. The resistors used in this circuit should be 1% metal-film type.

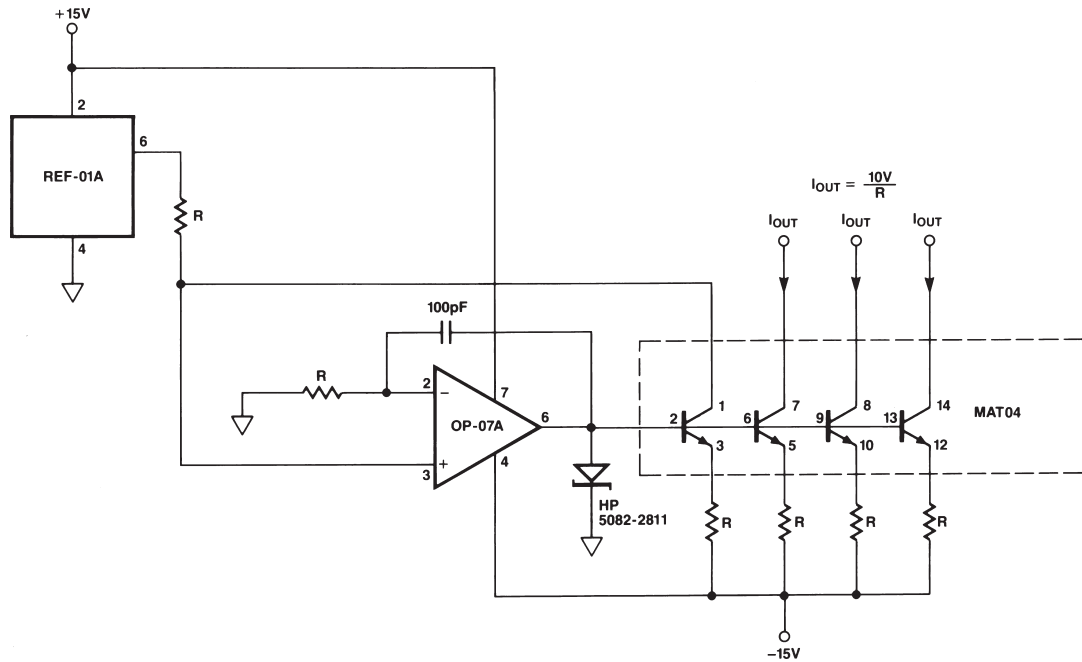


Figure 4. Temperature Independent Current Sink,  $I_{OUT} = 10\text{ V}/R\Omega$

**NONLINEAR FUNCTIONS**

An application where precision matched-transistors are a powerful tool is in the generation of nonlinear functions. These circuits are based on the transistor's logarithmic property, which takes the following idealized form:

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S}$$

The MAT04, with its excellent logarithmic conformance, maintains this idealized function over many decades of collector current. This, in addition to the stringent parametric matching of the MAT04, enables the implementation of extremely accurate log/antilog circuits.

The circuit of Figure 5 is a vector summer that adds and subtracts logged inputs to generate the following transfer function:

$$V_{OUT} = \frac{1}{\sqrt{2}} \sqrt{V_A^2 + V_B^2}$$

This circuit uses two MAT04 and maintains an accuracy of better than 0.5% over an input range of 10 mV to 10 V. The layout of the MAT04s reduces errors due to matching and temperature differences between the two precision quad matched transistors.

Op amps A1 and A2 translate the input voltages into logarithmic valued currents ( $I_A$  and  $I_B$  in Figure 5) that flow through transistor Q3 and Q5. These currents are summed by transistor Q4

$$(I_O = I_A + I_B = \sqrt{I_1^2 + I_2^2}),$$

which feeds the current-to-voltage converter consisting of op amp A3. To maintain accuracy, 1% metal-film resistors should be used.

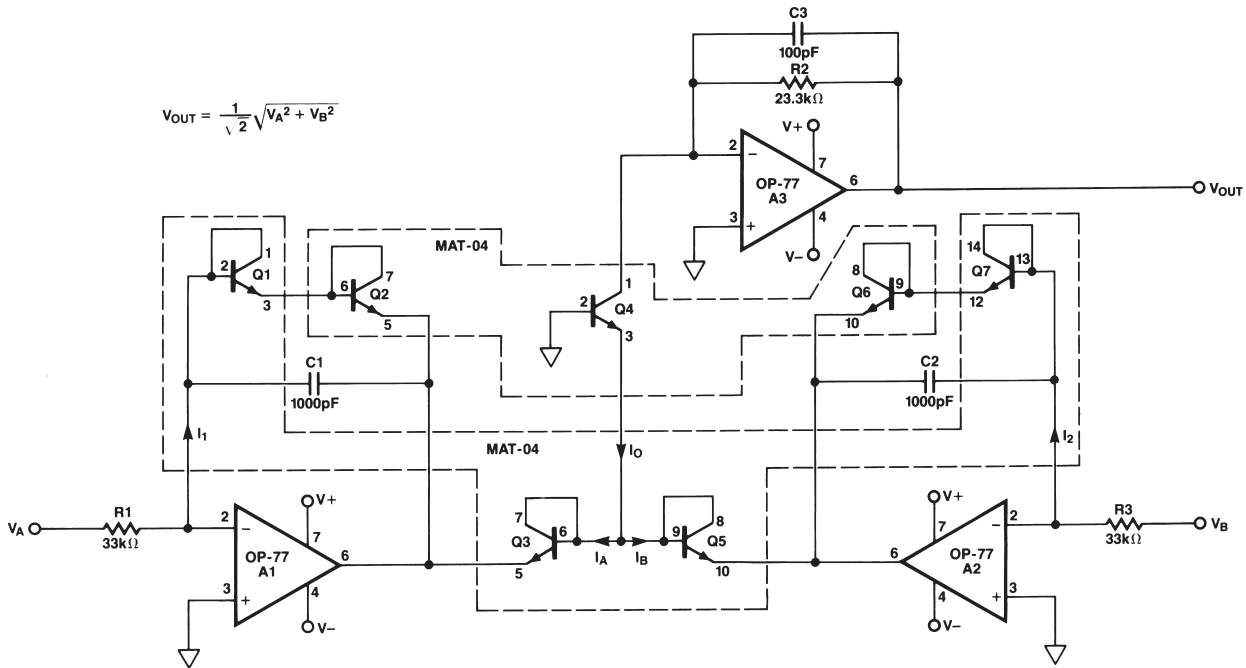


Figure 5. Vector Summer

**LOW NOISE, HIGH SPEED INSTRUMENTATION AMPLIFIER**

The circuit of Figure 6 is a very low noise, high speed amplifier, ideal for use in precision transducer and professional audio applications. The performance of the amplifier is summarized in Table I. Figure 7 shows the input referred spot noise over the 0–25 kHz bandwidth to be flat at 1.2 nV/√Hz. Figure 20 highlights the low 1/f noise corner at 2 Hz.

The circuit uses a high speed op amp, the OP17, preceded by an input amplifier. This consists of a precision dual matched-transistor, the MAT02, and a feedback V-to-I converter, the MAT04. The arrangement of the MAT04 is known as a “linearized cross quad” which performs the voltage-to-current conversion. The OP17 acts as an overall nulling amplifier to complete the feedback loop. Resistors R1, R2, and R3, R4 form voltage dividers that attenuate the output voltage swing since the “cross quad” arrangement has a limited input range. Biasing for the input stage is set by Zener diode Z1. At low currents, the effective zener voltage is about 3.3 V due to the soft knee characteristic of the Zener diode. This results in a bias current of 530 μA per side for the input stage. The gain of this amplifier with the values shown in Figure 6 is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{33000}{R_G}$$

Table I. Instrumentation Amplifier Characteristics

Input Noise Voltage Density	G = 1000	1.2 nV/√Hz
	G = 100	3.6 nV/√Hz
	G = 10	30 nV/√Hz
Bandwidth	G = 500	400 kHz
	G = 100	1 MHz
	G = 10	1.2 MHz
Slew Rate		40 V/μs
Common-Mode Rejection	G = 1000	130 dB
Distortion	G = 100	0.03%
	f = 20 Hz to 20 kHz	
Settling Time	G = 1000	10 μs
Power Consumption		350 mW



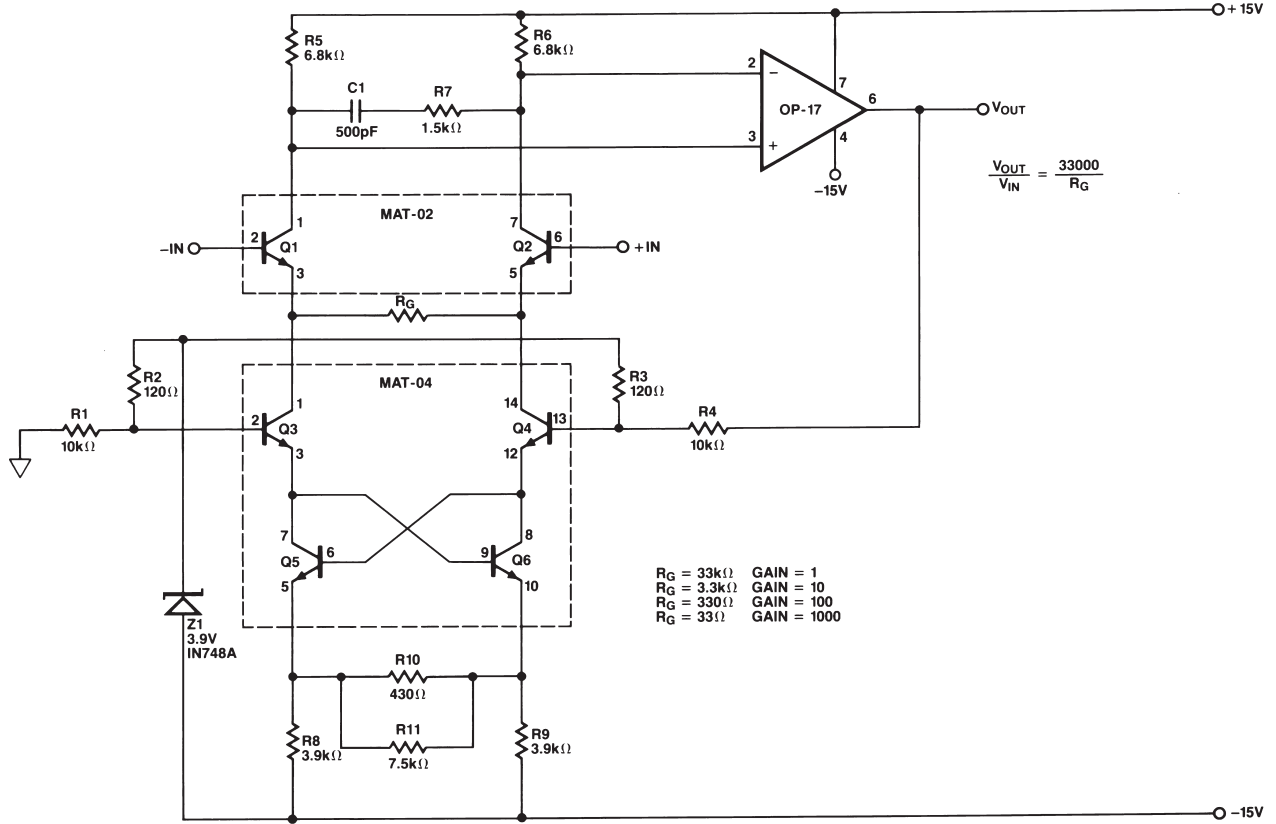
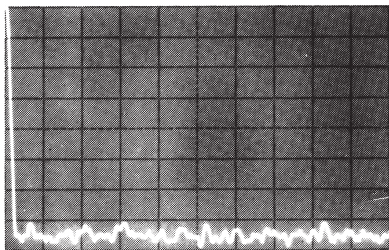
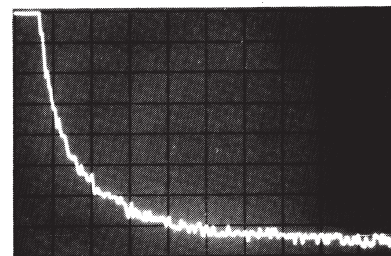


Figure 6. Low Noise, High-Speed Instrumentation Amplifier



NORMALIZED VERTICAL AXIS = 2.6nV/√ Hz /DIVISION  
REFERENCED TO INPUT.  
HORIZONTAL AXIS = 0 TO 25kHz.

Figure 7. Spot Noise of the Instrumentation Amplifier from 0–25 kHz, Gain Of 1000



HORIZONTAL AXIS = 0 TO 5Hz

Figure 8. Low Frequency Noise Spectrum Showing Low 2 Hz Noise Corner, Gain = 1000

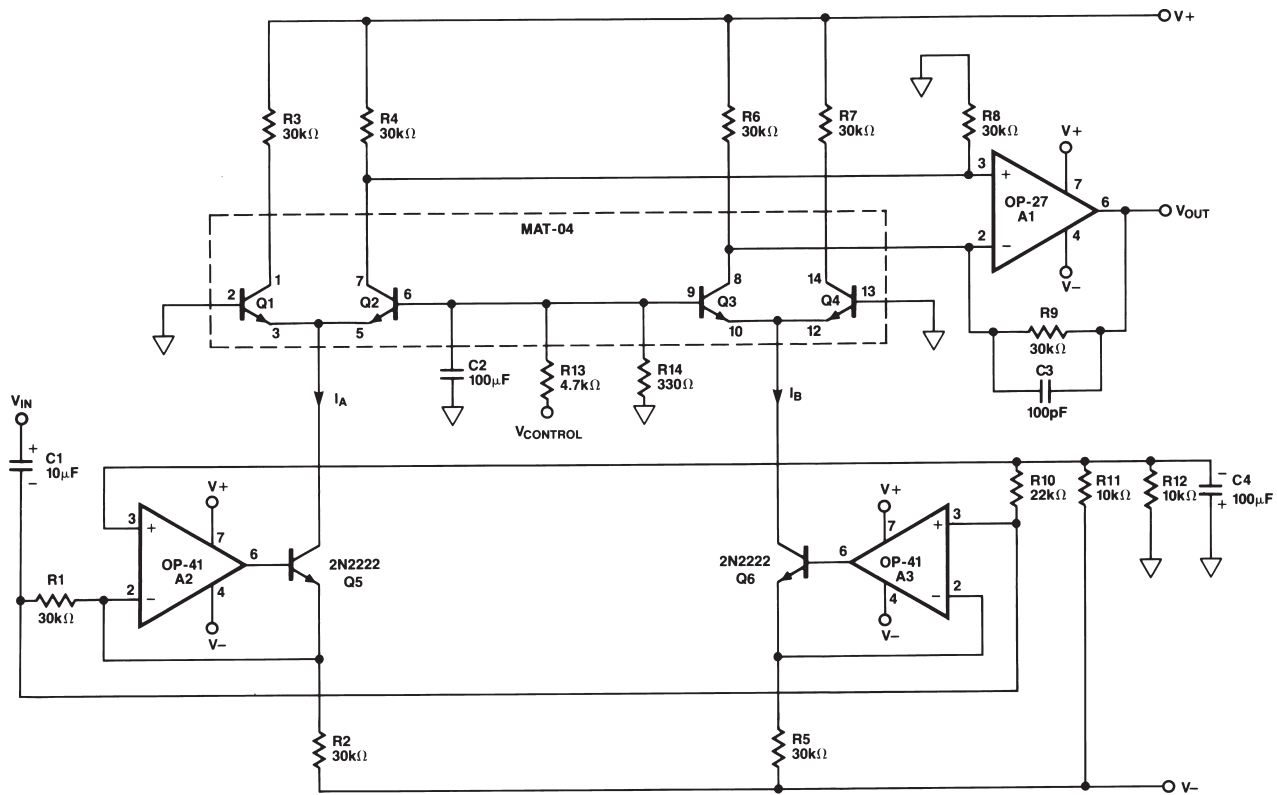


Figure 9. Voltage-Controlled Attenuator

**VOLTAGE-CONTROLLED ATTENUATOR**

The voltage-controlled attenuator (VCA) of Figure 9, widely used in professional audio circles, can easily be implemented using a MAT04. The excellent matching characteristics of the MAT04 enables the VCA to have a distortion level of under 0.03% over a wide range of control voltages. The VCA accepts a 3 V RMS input and easily handles the full 20 Hz–20 kHz audio bandwidth as shown in Figure 10. Noise level for the VCA is more than 110 dB below maximum output.

In the voltage controlled attenuator, the input signal modulates the stage current of each differential pair. Op amps A2 and A3 in conjunction with transistors Q5 and Q6 form voltage-to-current converters that transform a single input voltage into differential currents which form the stage currents of each differential pair. The control voltage shifts the current between each side of the two differential pairs, regulating the signal level reaching the output stage which consists of op amp A1. Figure 11 shows the increase in signal attenuation as the control voltage becomes more negative.

The ideal transfer function for the voltage-controlled attenuator is:

$$V_{OUT} / I_{IN} = \frac{2}{1 + \exp\left(V_{CONTROL}\right)\left(\frac{R14}{R13 + R14}\right)\left/\left(\frac{kT}{q}\right)\right)}$$

Where  $k$  = Boltzman constant  $1.38 \times 10^{-23} \text{J}/^\circ\text{K}$

$T$  = temperature in  $^\circ\text{K}$

$q$  = electronic charge =  $1.602 \times 10^{-19} \text{C}$

From the transfer function it can be seen that the maximum gain of the circuit is 2 (6 dB).

To ensure best performance, resistors R2 through R7 should be 1% metal film resistors. Since capacitor C2 can see small amounts of reverse bias when the control voltage is positive, it may be prudent to use a nonpolarized tantalum capacitor.

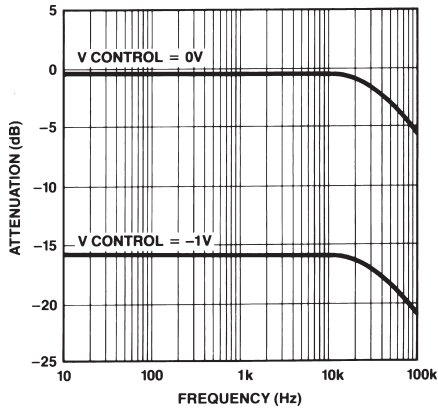


Figure 10. Voltage-Controlled Attenuator, Attenuation vs. Frequency

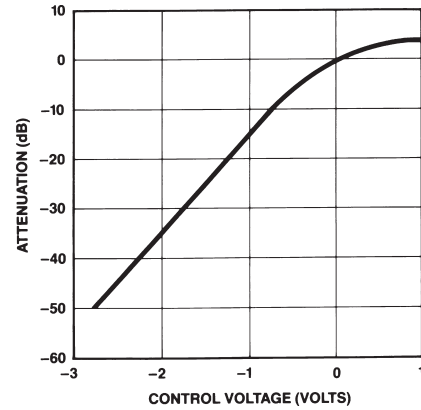
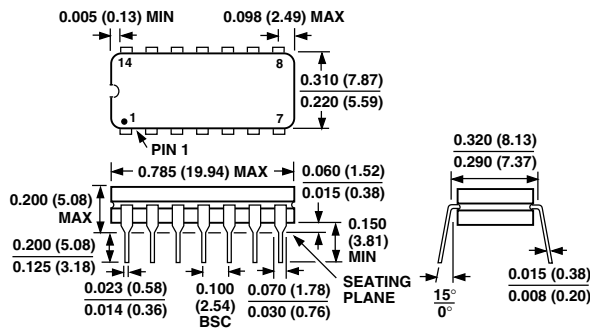


Figure 11. Voltage-Controlled Attenuator, Attenuation vs. Control Voltage

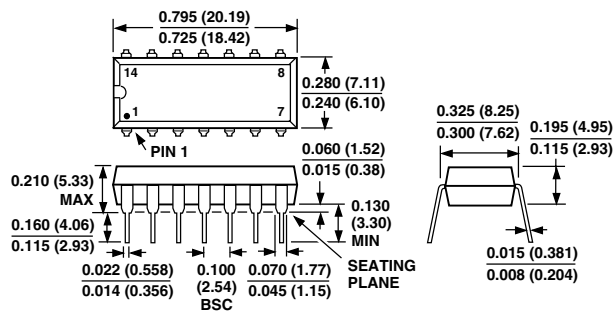
**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

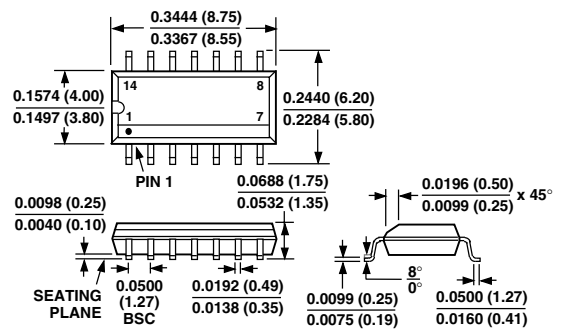
**14-Lead Cerdip (Q-14)**



**14-Lead Plastic DIP (N-14)**



**14-Lead Narrow-Body SO (R-14/SO-14)**



# MAT04

## Revision History

<b>Location</b>	<b>Page</b>
<b>Data Sheet changed from REV. C to REV. D.</b>	
Edits to ABSOLUTE MAXIMUM RATINGS .....	1
Deleted ELECTRICAL CHARACTERISTICS for -55°C .....	3
Deleted WAFER TEST LIMITS .....	4
Edits to TPCs .....	5-6
Added OUTLINE DIMENSIONS .....	13

C00285-0-2/02(D)

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